

AS
22. The process as claimed in claim 16, comprising
depositing the epitaxial layer in a deposition atmosphere
containing a deposition gas and a dopant gas, the deposition gas
being selected from the group of gases consisting of
trichlorosilane, silane, dichlorosilane, tetrachlorosilane and
mixtures of these gases; and the dopant gas is selected from the
group of gases consisting of diborane, phosphine and arsine.

23. The process as claimed in claim 16, comprising
depositing the epitaxial layer within a deposition time
of from 1 to 10 s.

24. The process as claimed in claim 16, comprising
cleaning the deposition reactor with an etching gas or
plasma at the earliest after an epitaxial layer has been deposited
on 50 substrate wafers in succession.

REMARKS

The amendments to this patent application are as follows. An
Abstract of the Disclosure on its own separate sheet has been
added. The Specification has been amended to include a cross
reference to related applications and to include changes made in
the International Office. The specification has also been amended
to include the section headings required by U.S. practice.
Amendments to the claims are to remove the multiple dependency of

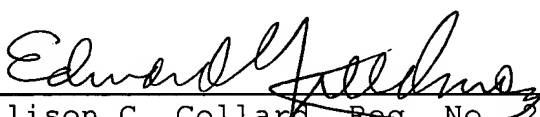
certain claims, and to include revisions made in the International Office.

No new matter has been introduced by this Amendment. Entry and consideration of this Amendment is respectfully requested.

Respectfully submitted,

Reinhard SCHAUER ET AL 1 PCT

By:


Allison C. Collard, Reg. No. 22,532
Edward R. Freedman, Reg. No. 26,048
Attorneys for Applicant

COLLARD & ROE, P.C.
1077 Northern Boulevard
Roslyn, NY 11576
(516) 365-9802

Encl.: 1. Abstract of the Disclosure
2. Marked-up Version of Pages 1, 2 and 6 of the Specification

Express Mail No. EL 871 446 549 US
Date of Deposit AUGUST 2, 2001

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10, on the date indicated above, and is addressed to the Ass't. Commissioner for Patents, Washington, D.C. 20231


Lisa L. Vulpis

0990656.080201

09/890656

JOJO Reg'd PCT/PTO 0 2 AUG 2001

MARKED-UP VERSION
OF SPECIFICATION

09890656-080201

09/890656
02 AUG 2001

Semiconductor wafer with a thin epitaxial layer, and

process for producing the semiconductor wafer

CROSS-REFERENCE TO RELATED APPLICATIONS

1. Field OF THE INVENTION

The invention relates to a semiconductor wafer with a
5 thin epitaxial layer, and a process for producing the
semiconductor wafer by depositing the layer on a
substrate wafer made of monocrystalline silicon.

2. The Prior Art

EP-829559 A1 discloses a process for producing
10 semiconductor wafers with a low defect density, it
being necessary to provide a single crystal which has
to be pulled with forced cooling or has to have a
specific oxygen and nitrogen concentration, and
semiconductor wafers obtained from the single crystal
15 having to be subjected to heat treatment. EP-644588 A1
relates to a semiconductor wafer having an epitaxially
provided layer which has a low defect density and
originates from a single crystal pulled at a pulling
rate of at most 0.6 mm/min.

20 At the present time intensive investigations are under
way with the aim of establishing which features
semiconductor wafers with an epitaxial layer have to
have in order to qualify them as a base material for
25 the production of modern CMOS components. According to
the publication in Jpn. J. Appl. Phys. Vol. 36 (1997),
pp. 2565-2570, a semiconductor wafer comprising a
p⁻-doped substrate wafer and a likewise p⁻-doped
epitaxial layer having a thickness of 1 μ m is
30 particularly suitable for large scale integrated CMOS
applications. This appraisal is also supported by the
publication in Electrochemical Society Proceedings
Volume 98-1, pp. 855-861. However, this paper also
draws attention to light-scattering defects (light
35 point defects) on the surface which occur in a
semiconductor wafer with a thin epitaxial layer but do
not adversely affect the GOI (gate oxide integrity).

09890656-080201

The abovementioned defects are called LLSs (localized light scatterers) by experts. Despite their indifferent behavior with regard to the GOI, the LLSs are undesirable to manufacturers of integrated circuits, which is also demonstrated by the fact that the ITRS (International Roadmap For Semiconductors) demands that the number of LLSs with a size of greater than or equal to $0.085 \mu\text{m}$ be less than or equal to 38 per semiconductor wafer with an epitaxial layer. This requirement applies to $0.18 \mu\text{m}$ technology and it must be assumed that as miniaturization advances ($0.13 \mu\text{m}$ and below), an even more stringent requirement will be imposed on the number of LLSs. Moreover, the limit value of 38 LLSs represents a maximum value and it should be taken into account that the number required for an industrial process capability must be significantly less than that.

SUMMARY OF THE INVENTION

The object of the invention was to provide a semiconductor wafer with an epitaxial layer which is suitable for modern CMOS applications, has a particularly small number of LLSs and requires comparatively low production costs. The object of the invention is, moreover, to specify a process for producing the semiconductor wafer.

The invention relates to a semiconductor wafer, comprising a substrate wafer made of monocrystalline silicon and an epitaxial layer deposited thereon, which is characterized in that the substrate wafer has a resistivity of from 0.1 to $50 \Omega\text{cm}$, an oxygen concentration of less than $7.5 \cdot 10^{17} \text{ atcm}^{-3}$ and a nitrogen concentration of from $1 \cdot 10^{13}$ to $5 \cdot 10^{15} \text{ atcm}^{-3}$, and the epitaxial layer has a thickness of from 0.2 to $1.0 \mu\text{m}$ and has a surface on which fewer than 30 LLS defects with a size of more than $0.085 \mu\text{m}$ can be detected.

After the deposition of the epitaxial layer, the semiconductor wafer, preferably in an atmosphere of hydrogen, is brought to a discharge temperature of preferably from 850 to 950°C and discharged from the deposition reactor.

It is possible to coat at least 50, preferably up to 200, substrate wafers in succession before the deposition reactor has to be cleaned with an etching gas or a plasma.

Semiconductor wafers produced according to the invention were compared with conventionally produced semiconductor wafers with regard to LLSs.

15 DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Example:

The semiconductor wafers produced according to the invention comprised a substrate wafer made of silicon with a resistivity of 12 Ωcm (p^- -type doping), on which an epitaxial layer having a layer thickness of 0.5 μm and a resistivity of 1.5 Ωcm had been grown. The deposition temperature was from 1130 to 1190°C. The substrate wafers were of type I and type II.

In the case of the conventionally produced semiconductor wafers, the substrate wafers originated from a single crystal pulled according to the Czochralski method without any doping with nitrogen. Substrate wafers from a single crystal pulled in this way are referred to below as reference I substrate wafers, if the single crystal had been cooled without forced cooling. In the case of the substrate wafers referred to as reference II substrate wafers, the corresponding single crystal was subjected to forced cooling. The epitaxial layer was deposited under the same conditions as those prevailing for the semiconductor wafers produced according to the invention.

09890656-080201